RS20N60D

N Channel MOSFET		(R) Lead Free Packa	age and Finish
Applications:		U III	C I
•PWM applications	lD	RDS(ON)(Max.)	Vdss
•Load switch	60A	6.5mΩ	20V
 Power management 			
Features: •VDS=20V; ID=60A RDS(ON) < 6.5mΩ @ VGS =4.5V Rds(on) < 10mΩ @ VGS =2.5V •Ultra Low On-Resistance •High UIS and UIS 100% Test •RoHS Compliant	TO-252(DPAK)	1.Gate o top view	2.Drain

Ordering Information

Part Number	Package	Marking
RS20N60D	TO-252	RS20N60D

Absolute Maximun Ratings Tc=25°C unless otherwise specified

Symbol	Parameter	RS20N60D	Units	
VDSS	Drain-to-Source Voltage	20	V	
ID	Continuous Drain Current (Tc=25°C)	60		
U	Continuous Drain Current Tc=100°C	39	А	
IDM	Pulsed Drain Current (Note*1)	240		
PD	Power Dissipation (Tc=25°C)	37	W	
VGS	Gate-to-Source Voltage	±20	V	
EAS	Single Pulse Avalanche Engergy (Note*2)	47.6	mJ	
	Maximum Temperature for Soldering			
TL TPKG	Leads at 0.063in(1.6mm)from Case for 10 seconds	300 260	°C	
	Package Body for 10 seconds		Ű	
TJ and TSTG	Operating Junction and Storage	-55 to 175		
	Temperature Range			

*Drain Current Limited by Maximum Junction Temperature

Caution:Stresses greater than those listed in the "Absolute Maximum Ratings" Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	RS20N60D	Units	Test Conditions
R0JC	Junction-to-Case	4	°C/W	Drain lead soldered to water cooled heatsink,PD adjusted for a peak junction temperature of +175℃.

OFF Characteristics TJ=25°C unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
BVDSS	Drain-to-source Breakdown Voltage	20			V	VGS=0V,ID=250µA
IDSS	Drain-to-Source Leakage Current			1	μA	VDS=20V,VGS=0V
IGSS	Gate-to-Source Forward Leakage			100	n۸	VGS=+12V VDS=0V
1000	Gate-to-Source Reverse Leakage			-100	nA	VGS=-12V VDS=0V

ON Characteristics TJ=25°C unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
RDS(on)	Static Drain-to-Source On-Resistance (Note*3)		4.8	6.5	mΩ	VGS=4.5V,ID=25A
KD3(0II)			6.8	10.0	mΩ	VGS=2.5V,ID=15A
VGS(TH)	Gate Threshold Voltage	0.4	0.7	1.0	V	VGS=VDS,ID=250µA

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
td(ON)	Turn-on Delay Time		15			VDS=10V
trise	Rise Time		37		nS	VGS=4.5V
td(OFF)	Turn-OFF Delay Time		52		115	ID=25A RG=3Ω
tfall	Fall Time		21			κ σ= 3Ω

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions	
Ciss	Input Capacitance		1799			VGS=0V	
Coss	Output Capacitance		298		pF	VDS=10V	
Crss	Reverse Transfer Capacitance		283			f=1.0MHz	
Qg	Total Gate Charge		23			VDS=10V ID=25A	
Qgs	Gate-to-Source Charge		5		nC		
Qgd	Gate-to-Drain("Miller")Charge		7			VGS=4.5V	

Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
ISD	Source-Drain Current(Body Diode)			60	А	
ISDM	Pulsed Source-Drain Current(Body Diode)			240	Δ	Maximum Pulsed Drain to Source Diode Forward Current
Vsd	Diode Forward Voltage			1.3	V	IS=30A,VGS=0V
trr	Reverse Recovery Time		25		nS	VGS=0V
Qrr	Reverse Recovery Charge		21		nC	IF=25A,di/dt=100A/µs

Notes:

- *1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
- *2. EAS condition: TJ=25 $^{\circ}$ C, VDD=10V, VG=4.5V, L=0.5mH, RG=25 Ω , IAS=13.8A
- *3. Pulse Test: Pulse Width ≤300µs, Duty Cycle ≤0.5%

Typical Feature curve

Figure 1. Output Characteristics (TJ = 25°C)

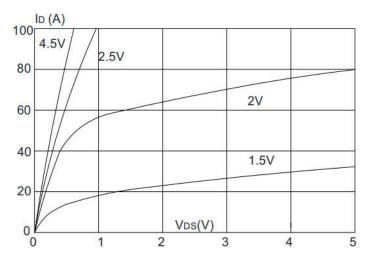


Figure 2. Transfer Characteristics

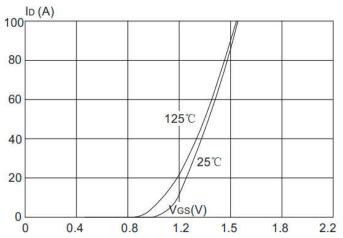


Figure 3. On-Resistance vs. Drain Current

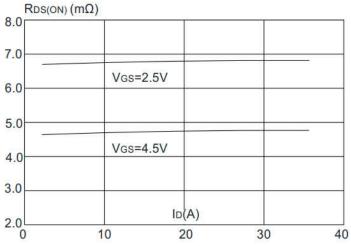
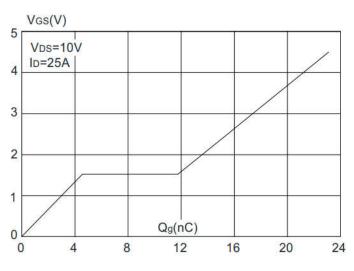


Figure 5. Gate Charge Characteristics





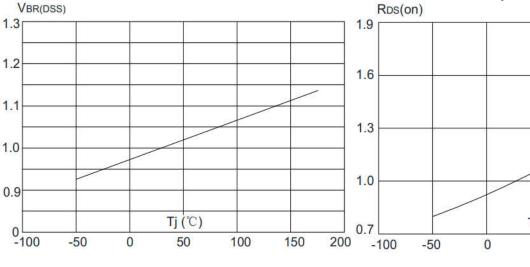


Figure 4: Body Diode Characteristics

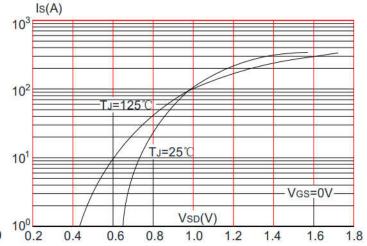
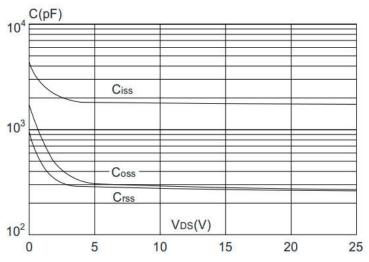
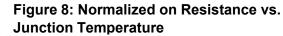
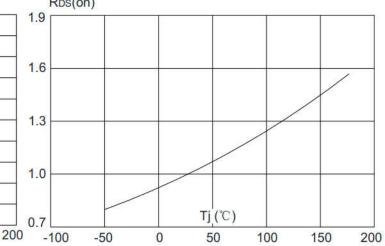


Figure 6. Capacitance Characteristics







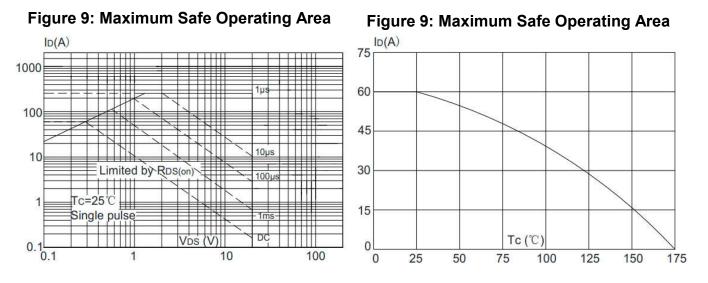
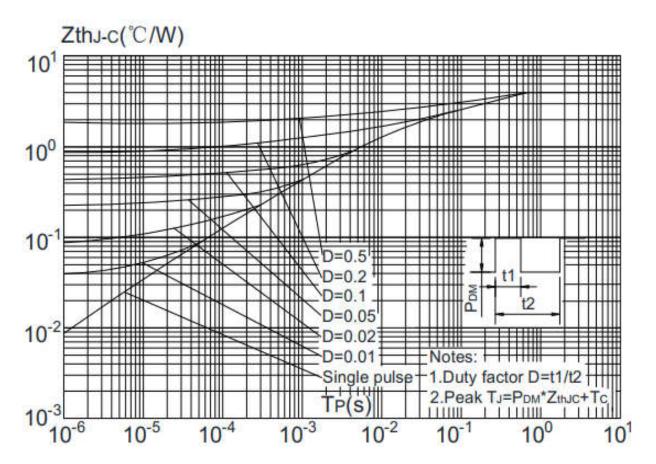
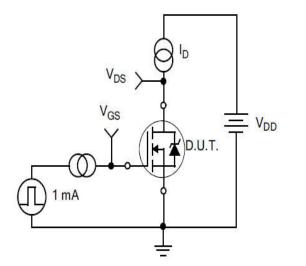


Figure.11: Maximum Effective Transient Thermal Impedance, Junctionto-Case



Test Circuits and Waveforms



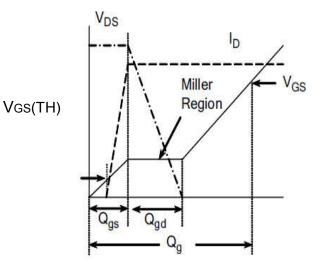


Figure A. Gate Charge Test Circuit

Figure B. Gate Charge Waveform

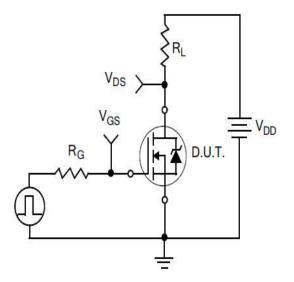


Figure C. Resistive Switching Test Circuit

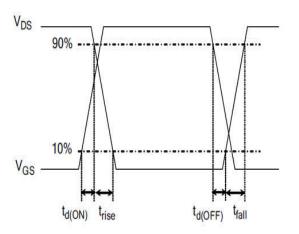
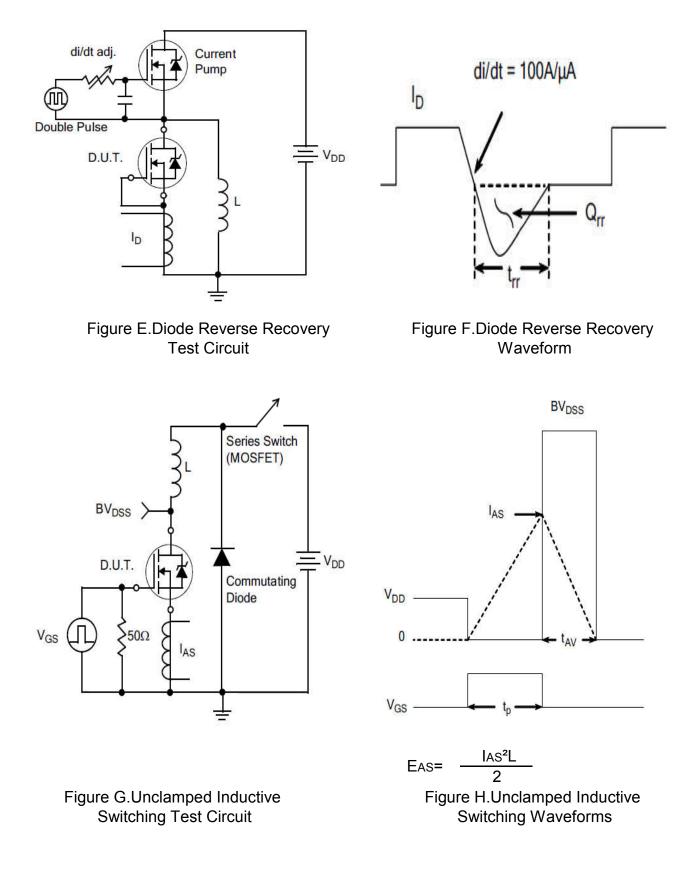


Figure D. Resistive Switching Waveforms

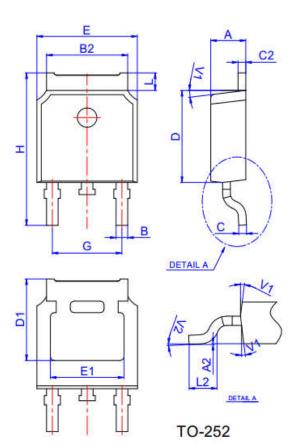
http://www.reasunos.com

Test Circuits and Waveforms



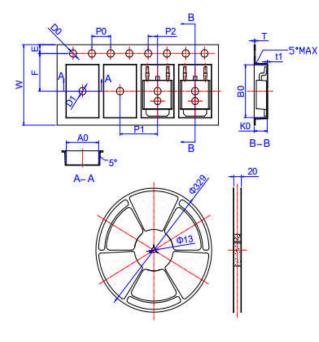
http://www.reasunos.com

Package outline drawing



	Dimensions								
Ref.		Millimete	ers	Inches					
	Min.	Тур.	Max.	Min.	Тур.	Max.			
А	2.10		2.50	0.083		0.098			
A2	0		0.10	0		0.004			
в	0.66		0.86	0.026		0.034			
B2	5.18		5.48	0.202		0.216			
С	0.40		0.60	0.016		0.024			
C2	0.44		0.58	0.017		0.023			
D	5.90		6.30	0.232		0.248			
D1		5.30RE	0	0.209REF					
Е	6.40		6.80	0.252		0.268			
E1	4.63			0.182					
G	4.47		4.67	0.176		0.184			
н	9.50		10.70	0.374		0.421			
L	1.09		1.21	0.043		0.048			
L2	1.35		1.65	0.053		0.065			
V1		7°			7°				
V2	0°		6°	0°		6°			

Reel Spectification-TO-252



	Dimensions									
Ref.		Millimete	rs	Inches						
	Min.	Тур.	Max.	Min.	Тур.	Max.				
w	15.90	16.00	16.10	0.626	0.630	0.634				
E	1.65	1.75	1.85	0.065	0.069	0.073				
F	7.40	7.50	7.60	0.291	0.295	0.299				
D0	1.40	1.50	1.60	0.055	0.059	0.063				
D1	1.40	1.50	1.60	0.055	0.059	0.063				
P0	3.90	4.00	4.10	0.154	0.157	0.161				
P1	7.90	8.00	8.10	0.311	0.315	0.319				
P2	1.90	2.00	2.10	0.075	0.079	0.083				
AO	6.85	6.90	7.00	0.270	0.271	0.276				
B0	10.45	10.50	10.60	0.411	0.413	0.417				
К0	2.68	2.78	2.88	0.105	0.109	0.113				
Т	0.24		0.27	0.009		0.011				
t1	0.10			0.004						
10P0	39.80	40.00	40.20	1.567	1.575	1.583				

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